```
File   2:INSPEC 1969-2004/May W2
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         (c) 2004 TWI Ltd
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         (c) 2004 The HW Wilson Co.
File 103:Energy SciTec 1974-2004/May B1
         (c) 2004 Contains copyrighted material
File 144:Pascal 1973-2004/May W2
         (c) 2004 INIST/CNRS
File 239:Mathsci 1940-2004/Jun
         (c) 2004 American Mathematical Society
File 241:Elec. Power DB 1972-1999/Jan
         (c) 1999 Electric Power Research Inst.Inc
File 305:Analytical Abstracts 1980-2004/May W2
         (c) 2004 Royal Soc Chemistry
File 315:ChemEng & Biotec Abs 1970-2004/Apr
         (c) 2004 DECHEMA
File 987:TULSA (Petroleum Abs) 1965-2004/May W4
         (c)2004 The University of Tulsa

Set     Items   Description
S1     170366   BALL? ? OR BUMP?
S2       7983   BLM OR BALL(W)LIMIT? OR UBM OR UNDERBUMP? OR UNDER(W)BUMP?
S3    2712914   WINDOW? OR ACCESS? OR HOLE? OR OPEN?
S4    3065033   PLASMA? ? OR IONIS? OR IONIZ? OR CLEAN????
S5          2   S2 AND S3(4N)S4
S6          2   S1 AND S2 AND S3 AND S4
S7          2   S6 NOT S5
S8          1   RD (unique items)
S9         41   S1(3N)SOLDER? AND  S3 AND S4
S10        32   S9 NOT S5:S6 NOT PY>2002
S11        28   RD (unique items)
Temp SearchSave "TD290" stored
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File 342:Derwent Patents Citation Indx 1978-04/200427
       (c) 2004 Thomson Derwent

      Set  Items  Description
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? s pn=(us 5656858)      <<KONDO ET AL>>
      S1       1  PN=(US 5656858)
? map pn t ex            <<all patents in KONDO family>>
Serial#TD293
       S2       1  Serial: TD293
? map ct t ex /pn=
Serial#TD294             <<patents cited in KONDO>>
      S3       4  Serial: TD294
? map cg t ex
Serial#TD295             <<patents citing patents cited in KONDO>>
      S4     291  Serial: TD295
? map anpr t
Serial#TD296             <<application numbers of S4>>

File 350:Derwent WPIX 1963-2004/UD,UM &UP=200431
         (c) 2004  Thomson Derwent

Set     Items   Description
S1        967   Serial: TD296
S2     116541   BALL? ? OR BUMP? OR SOLDER?
S3        414   BLM OR BALL(W)LIMIT? OR UBM OR UNDERBUMP? OR UNDER(W)BUMP?
S4     458720   PLASMA? ? OR CLEAN???? OR IONIS? OR IONIZ?
S5    1997730   WINDOW? OR ACCESS? OR HOLE? OR OPEN?
S6        726   BENZOCYCLOBUTENE? OR CYCLOTENE?
S7          0   S1 AND S2 AND S4 AND S6
S8          9   S1 AND S4 AND S5
S9         45   S1 AND S2:S3 AND S5
S10        43   S9 NOT S8
S11         1   S10 AND S6
S12       831   S6 OR BCB
S13   1395321   POLYMR OR POLYMER? OR POLY OR POLYBEZOXAZOL? OR S12
S14        13   S10 AND S13
? map anpr t
Serial#TD297

File 342:Derwent Patents Citation Indx 1978-04/200427
       (c) 2004 Thomson Derwent

Set     Items   Description
S1         52   Serial: TD297
? map pn t ex /ct=
      Serial#TD298       <<patents that cite the patents in S14, above>>
S2        628   Serial: TD298
S3     621  S2 NOT S1
? map anpr t
Serial#TD301
Serial#TD302
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File 350:Derwent WPIX 1963-2004/UD,UM &UP=200431
         (c) 2004  Thomson Derwent

Set     Items   Description
S1         90   Serial: TD302
S2       2602   Serial: TD301
S3       2647   S1:S2         <<patents that cite the patents in S14, above>>
S4        414   BLM OR BALL(W)LIMIT? OR UBM OR UNDERBUMP? OR UNDER(W)BUMP?
S5     458720   PLASMA? ? OR CLEAN???? OR IONIS? OR IONIZ?
S6    1997730   WINDOW? OR ACCESS? OR HOLE? OR OPEN?
S7    1395321   BENZOCYCLOBUTENE? OR CYCLOTENE? OR BCB OR POLYMR OR POLYMER? OR POLY
                  OR POLYBEZOXAZOL?
S8          0   S3 AND S4 AND S5 AND S6 AND S7
S9     277973   BALL? ? OR BUMP? OR SOLDER?
S10        39   (S9 OR S4) AND S3 AND S5:S6 AND S7
? save temp
Temp SearchSave "TD303" stored
```

12/17/04

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 3/15/2004 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, JEF-4B68, 272-2511.

Date 5/17/04 Serial # 10/086,117 Priority Application Date _____

Your Name M. Lewis Examiner # _____

AU 2822 Phone 272-1738 Room 5A30

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

05-17-04 P03:23

Where have you searched so far on this case?
Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other _____
Secondary Refs ✓ Foreign Patents ___
Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-11, 19-25

Problem: See page 1-4

Solution: " " 5-7

US 5,676,858 1°
" 6,133,136 1°
" 5,016,389 2°
" 2002/0096764 2°

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Searcher Phone: 2-2663
Searcher Location: STIC-EIC2800, JEF-4B68
Date Searcher Picked Up: 5/19/4
Date Completed: 5/21/4
Searcher Prep/Rev Time: 5/0 53
Online Time: _____

Type of Search

Structure (#)_____
Bibliographic ✓
Litigation_____
Fulltext_____
Patent Family_____
Other_____

Vendors

STN ✓
Dialog ✓
Questel/Orbit_____
Lexis-Nexis_____
WWW/Internet_____
Other _____

7/5/1 (Item 1 from file: 2)
DIALOG(R)File 2:**INSPEC**

6729541 INSPEC Abstract Number: B2000-11-0170J-126
Title: **UBM** formation on single die/dice for flip chip applications
Author(s): Jittinorasett, S.; Barlow, F.; McGrath, J.; Elshabini, A.
Author Affiliation: Dept. of Electr. Eng./HiDEC, Arkansas Univ., Fayetteville, AR, USA
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.3906 p.39-44
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1999 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
Conference Date: 26-28 Oct. 1999 Conference Location: Chicago, IL, USA
Abstract: Flip chip bonding is well known to have many advantages and it has been used for many applications in the electronic packaging industry to achieve high I/O count and high electrical performance. Currently, **Under Bump** Metallurgy (**UBM**) is one of the most important methodologies to obtain reliable connections in the solder **bump** structure of the Flip Chip. **UBM** can be deposited on wafers through various techniques such as sputtering, evaporation, or electroless plating. However, these processes are only suitable for very high volume production, but in general, they are not practical for use in prototyping stages or in low volume production, especially where the entire wafer is not readily **accessible**. This paper reports a low cost **UBM** deposition process for use on a single die or a number of dice. This new technique will allow Flip Chip bonding to be based on a single die and will be suitable for low volume applications. The **UBM** deposition process on aluminum pads of a single die consists of two major processing steps. Firstly, step one temporarily attaches the die to a substrate using an amorphous thermoplastic adhesive. Such adhesives may be **cleanly** removed from the die backside, with suitable solvents, after the **UBM** deposition is achieved. The second step is to deposit the **UBM** layer using nickel electroless plating. A zincation process is performed to pretreat the aluminum surface prior to the plating process. This paper will discuss in details the procedures used in each process step as well as the experimental results and the analysis of data for the newly developed process. (11 Refs)
Subfile: B
Descriptors: adhesives; electroless deposition; flip-chip devices; integrated circuit metallisation; integrated circuit packaging; soldering; wafer bonding
Identifiers: **UBM** formation; flip chip applications; electronic packaging industry; **under bump** metallurgy; solder **bump** structure; low volume production; single die; amorphous thermoplastic adhesive; electroless plating; zincation process; Ni
Class Codes: B0170J (Product packaging); B0520J (Deposition from liquid phases); B0170G (General fabrication techniques); B2240 (Microassembly techniques)

11/5/2 (Item 2 from file: 2)
DIALOG(R)File 2:**INSPEC**

7411356 INSPEC Abstract Number: B2002-11-2570-007
Title: Stencil printing process of buffer layer for wafer level CSP
Author(s): Ezawa, H.; Seto, M.; Miyata, M.; Tazawa, H.
Conference Title: Proceedings 2001 International Symposium on Microelectronics (SPIE Vol.4587) p.95-9
Publisher: IMAPS - Int. Microelectron. & Packaging Soc, Washington, DC, USA
Publication Date: 2001 Country of Publication: USA xix+782 pp.
ISBN: 0 930815 64 5 Material Identity Number: XX-2002-00865
Conference Date: 9-11 Oct. 2001 Conference Location: Baltimore, MD
Abstract: We have confirmed that stencil printing, using a novel developed printable polyimide paste containing no fillers, can be used for polymer film deposition in wafer level chip size packaging (WLCSP) processes. A thick polyimide buffer layer with **openings** for **solder ball bumping** can be deposited on all of the LSIs on a wafer by a one time printing process. This stencil printing process does not need an expensive lithography tool and photoresist process, which makes WLCSP more cost effective than ever. In this study, the rheology of the polyimide paste was tailored to the stencil printing process. The novel printable polyimide paste shows a viscosity ratio of more than 3.95 to 1 at the shear rate of 1 s/sup -1/ to 10 s/sup -1/ respectively, and that viscosity of the paste goes up quickly after the shear rate is lowered rapidly. Fine spaces of 40 mu m between 250 mu m **openings** were obtained when the new paste was applied to deposit 10 mu m thick buffer films on Si wafers. It has been also confirmed that the new paste showed robust stability of viscosity after more than 100 wafers were continuously printed, leading to a narrow variation range of 30 mu m at the **opening** size of 385 mu m within 100 wafers. As for the adhesion and reliability of the printed polyimide films, no peelings were observed on **plasma** CVD SiN films after 300 hours under the PCT condition of 127 degrees C, 100% humidity and 0.25 MPa. This optimal stencil printing process using the novel developed paste will lead to higher productivity and, thus, to a significant cost reduction of WLCSP. (2 Refs)
Subfile: B
Descriptors: adhesion; chip scale packaging; insulating thin films; integrated circuit manufacture; integrated circuit reliability; large scale integration; polymer films; printing; rheology; viscosity; wafer-scale integration
Identifiers: wafer level CSP; buffer layer stencil printing process; printable polyimide paste; no-filler paste; polymer film deposition; WLCSP process; **solder ball bump openings**; wafer LSI; Si wafer buffer films; one time printing process; lithography tools; photoresist process; polyimide paste rheology; paste viscosity ratio; shear rate; robust viscosity stability; continuous wafer printing; **opening** size variation range; film adhesion; film reliability; film peeling; **plasma** CVD SiN films; PCT conditions; film temperature; film humidity conditions; high productivity printing; low cost printing process; 40 micron; 250 micron; 10 micron; 385 micron; 300 hr; 127 degC; Si; SiN
Class Codes: B2570 (Semiconductor integrated circuits); B0170E (Production facilities and engineering); B0170N (Reliability); B0170J (Product packaging); B0560 (Polymers and plastics (engineering materials science)); B2830C (Organic insulation)

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10/9/5

DIALOG(R)File 350:Derwent **WPIX**

016020211 **Image available**

WPI Acc No: 2004-178062/200417

Semiconductor chip assembly comprises has interlocking conductive traces

Patent Assignee: LIN C W C (LINC-I)

Inventor: LIN C W C

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6653742	**B1**	**20031125**	**US 2000687619**	**A**	**20001013**	**200417**	**B**
			US 2001878626	A	20010611		
			US 2001939140	A	20010824		
			US 2002235331	A	20020905		

CIP of patent **US 6440835**

Abstract (Basic): US 6653742 B1

NOVELTY - A semiconductor chip assembly comprises an insulative adhesive that contacts a chip, first and second surfaces and outer edges of a conductive trace, where the insulative adhesive extends completely across the second surface between the outer edges, extends completely across the outer edges between the first and second surfaces, and extends partially but not completely across the first surface between the outer edges.

DETAILED DESCRIPTION - A semiconductor chip assembly comprises a semiconductor chip with a conductive pad; a conductive trace that includes a first surface, a second surface opposite the first surface, and elongated outer edges between the first and second surfaces, where the first surface faces away from the chip and the second surface faces towards the chip; an insulative adhesive that contacts the chip, the first and second surfaces and the outer edges, where the insulative adhesive extends completely across the second surface between the outer edges, extends completely across the outer edges between the first and second surfaces, and extends partially but not completely across the first surface between the outer edges; and a connection joint that contacts and electrically connects the conductive trace and the pad.

An INDEPENDENT CLAIM is also included for making a semiconductor chip assembly, comprising providing a metal base with first and second opposing surfaces; providing a first plating mask on the first surface of the metal base, where the first plating mask includes an **opening** that exposes a portion of the first surface; electroplating a first metal pattern on the exposed portion of the first surface through the **opening** in the first plating mask, where the first metal pattern includes a first metal layer and a second metal layer, the first metal layer contacts the metal base and has a different composition than the metal base, and the second metal layer is separated from the metal base; removing the first plating mask, exposing outer edges of the first metal pattern; providing a second plating mask on the second surface of the metal base, where the second plating mask includes an **opening** that exposes a portion of the second surface; electroplating a second metal pattern on the exposed portion of the second surface through the **opening** in the second plating mask, where the second metal pattern includes a third metal layer and a fourth metal layer, the third metal layer contacts the metal base and has a different composition than the metal base, and the fourth metal layer is separated from the metal base; removing the

second plating mask, exposing outer edges of the second metal pattern; mechanically attaching a chip to the second metal pattern using an insulative adhesive, where the chip includes a pad; forming an encapsulant that contacts the second surface of the metal base outside the periphery of the chip; applying an etch that is selective of the metal base with respect to the first and second metal layers using the first metal pattern as an etch mask, removing a portion of the metal base within the periphery of the chip without removing a portion of the metal base outside the periphery of the chip, forming a pillar in the metal base outside the periphery of the chip and exposing the second metal pattern; applying an etch that is selective of the adhesive with respect to the second metal pattern and the pad, removing a portion of the adhesive and exposing the pad; and forming a connection joint that contacts and electrically connects the second metal pattern and the pad.

USE - Used as chip scale packages, chip size packages, or **ball** grid arrays, useful for an electronic system.

ADVANTAGE - The chip assembly is devoid of wire bonds, tape automated bonding leads, and **solder** joints. It can be manufactured using low temperature processes which reduces stress and improves reliability, using well-controlled wet chemical processes, which can be easily implemented by circuit board, lead frame, and tape manufacturers, and using materials that are compatible with copper chip and lead-free environmental requirements. The conductive trace can be interlocked by the adhesive and/or encapsulant. The pillar can be formed using etching rather than by electroplating or electroless plating, which improves uniformity and reduces manufacturing time and cost.

DESCRIPTION OF DRAWING(S) - The figure is a top plan view of routing line variation.

pp; 58 DwgNo 13/13

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Component: The adhesive defines a gap that traverses the first surface and is centered between the outer edges. The gap traverses all of a length of the conductive trace. The adhesive is sandwiched between the conductive trace and the pad, and the connection joint contacts a surface of the conductive trace that overlaps and faces away from the pad. The connection joint contacts the first surface and the outer edges, and overlaps the pad.

POLYMERS - Preferred Material: The adhesive is a thermosetting epoxy or a thermosetting **polyimide**.

Title Terms: SEMICONDUCTOR; CHIP; ASSEMBLE; COMPRISE; INTERLOCKING; CONDUCTING; TRACE
Derwent Class: A85; L03; U11
International Patent Class (Main): H01L-023/48
International Patent Class (Additional): H01L-021/44
File Segment: CPI; EPI
Manual Codes (CPI/A-N): A11-C01C; A12-E04; A12-E07C; L04-C17D
Manual Codes (EPI/S-X): U11-D03C1; U11-E01; U11-E02A3

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10/9/7

DIALOG(R)File 350:Derwent **WPIX**

015995762 **Image available**

WPI Acc No: 2004-153612/200415
Fabrication of **solder bump** for flip-chip devices for limiting pad designs comprises providing **under bump** metal over substrate with exposed pad.
Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)
Inventor: CHEN L; CHEN Y; CHING K; LEE H; LIN C; SU C

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6602775	**B1**	**20030805**	**US 2001930677**	**A**	**20010816**	**200415**	**B**

Abstract (Basic): US 6602775 B1

NOVELTY - A **solder bump** is fabricated by providing an **under bump** metal (**UBM**) (16) over a substrate having an exposed pad (12). The **UBM** is in electrical contact with the pad.

DETAILED DESCRIPTION - Fabrication of a **solder bump** comprises:

(a) providing an **under bump** metal (**UBM**) over a substrate having an exposed pad;

(b) forming a first patterning layer (18') over the **UBM**;

(c) forming a second patterning layer over the first patterning layer;

(d) selectively exposing the first patterning layer with a light having a first wavelength, leaving a first unexposed portion centered over the pad between the first exposed portions;

(e) selectively exposing a second patterning layer (20, 20') with light having a second wavelength, leaving a second unexposed portion wider than and centered over the first unexposed portion of the exposed first patterning layer;

(f) removing the second unexposed portion of the exposed second patterning layer and the first unexposed portion of the exposed first patterning layer to form **opening**;

(g) forming a **solder** plug (32) within the **opening**;

(h) removing the exposed portions of the exposed first patterning layer and the exposed portions of the exposed second patterning layer; and

(i) reflowing the **solder** plug to form a **solder bump**.

The **UBM** is in electrical contact with the pad.

USE - Fabricating a **solder bump** for flip-chip devices used in limiting pad designs.

ADVANTAGE - The process improves the **bump** height without changing the **UBM** size (width). It is able to increase the **bump** height for a small pad design. It also achieves an improved **bump** height control. It improves the reliability of the flip-chip package and it prevents chip cracking.

DESCRIPTION OF DRAWING(S) - The figures illustrates the fabrication of **solder bump**.

Pad (12)
UBM (16)
Patterning layers (18', 20, 20')
Second patterned mask (26)
Solder plug (32)
pp; 9 DwgNo 3, 4, 7/8

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The **UBM** not under the **solder** ply before reflowing the **solder** plug. A passivation layer is formed over the substrate and the pad and is

etched to expose the pad. The first and second patterning layers are formed by a spin coating method.

Preferred Material: The first patterning layer is made of dry film resist, spin coated photoresist or negative spin coated photoresist. The second patterning layer is made of a negative spin coated photoresist or negative photosensitive dry film.

INORGANIC CHEMISTRY - Preferred Material: The pad is made of copper (Cu) or aluminum (Al)-Cu. The passivation layer is formed of silicon nitride and/or silicon dioxide. The **UBM** is made of titanium (Ti)/Cu, chromium/Cu, Al/nickel (Ni)/vanadium or Ti/Ni. The **solder** plug is made of tin-lead, lead-free material, tin-silver, tin-bismuth or silicon-zinc.

POLYMERS - Preferred Material: The passivation layer is formed of **polyimide** or **benzocyclobutene.**

Title Terms: FABRICATE; **SOLDER**; **BUMP**; FLIP; CHIP; DEVICE; LIMIT ; PAD; DESIGN; COMPRISE; **BUMP**; METAL; SUBSTRATE; EXPOSE; PAD
Derwent Class: A85; L03; U11; V04
International Patent Class (Main): H01L-021/44
File Segment: CPI; EPI
Manual Codes (CPI/A-N): A12-E07C; L04-C11C; L04-C17A
Manual Codes (EPI/S-X): U11-D03B1; U11-E01C; V04-R04A
Polymer Indexing (PS):
<01>
001 2004; P1081-R F72 D01
002 2004; ND01; K9416; K9552 K9483; Q9999 Q7454 Q7330

+=
10/9/10
DIALOG(R)File 350:Derwent **WPIX**

015667489 **Image available**
WPI Acc No: 2003-729676/200369
Manufacture of semiconductor chip assembly comprises providing semiconductor chip, providing support circuit, mechanically attaching chip to support circuit, exposing pad, and electrolessly plating contact terminal
Patent Assignee: LIN C W C (LINC-I)
Inventor: LIN C W C

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6562657	**B1**	**20030513**	**US 2000643214**	**A**	**20000822**	**200369**	**B**

Abstract (Basic): US 6562657 B1

NOVELTY - A semiconductor chip assembly is manufactured by providing semiconductor chip that includes conductive pad (16); providing support circuit that includes insulative base, conductive trace (28), and through **hole** (30); mechanically attaching chip to support circuit, exposing the pad using the through **hole,** and electrolessly plating contact terminal over first plating region.

DETAILED DESCRIPTION - The manufacture of semiconductor chip assembly involves providing semiconductor chip that includes conductive pad; providing support circuit that includes insulative base, conductive trace, and through **hole**; mechanically attaching chip to support circuit, exposing the pad using the through **hole,** and electrolessly plating contact terminal over first plating region and connection joint between second plating region and the pad without electrolessly plating a top sidewall portion. The support circuit

includes top and bottom surfaces. The through-**hole** includes top sidewall portion adjacent to the top surface and a bottom sidewall portion adjacent to the bottom surface. The conductive trace includes first plating region at the top surface and second plating region at the bottom sidewall portion.

USE - Used to manufacture semiconductor chip assembly.

ADVANTAGE - The invention is cost-effective, reliable, manufacturable, provides excellent mechanical and electrical performance, and complies with stringent environmental standards.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view showing a method of manufacturing the semiconductor chip assembly.

Pad (16)
Top surface (22)
Conductive trace (28)
Through-**hole** (30)
Plating region (40)
pp; 19 DwgNo 1G/3

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - The contact terminal is initially plated on the first plating region and a first portion of the connection joint on the second plating region and a second portion of the connection joint on the pad such that these first and second portions do not contact one another so as not to connect the second plating region to the pad and then electrolessly plating the contact terminal on the first plating region and the first portion on the second plating region and the second portion on the pad such that these portions contact one another to connect the second plating region to the pad. Metal is used during electroplating. An insulative adhesive is contacted to an upper surface of the chip. Exposing the pad includes etching. Preferred Components: The conductive trace includes a *pillar* and a routing line. The pillar extends above the base and is spaced from the through-**hole**. The top sidewall portion is formed in the base alone and is devoid of metal after plating. The sidewall portion is formed in the conductive trace alone. The conductive trace and connection joint provide all horizontal and vertical routing between the contact terminal and the pad. The assembly is a chip size package.

METALLURGY - Preferred Material: The contact terminal and connection joint include metal consisting of *copper*, gold, nickel, palladium, tin, and/or their alloys. The conductive trace includes copper. The connection joint consist of bottom layer having copper; middle layer having nickel; and top layer having palladium or **solder**.

POLYMERS - Preferred Material: The base is an insulator consisting of tape, epoxy, silicone, glass, or ceramic

Title Terms: MANUFACTURE; SEMICONDUCTOR; CHIP; ASSEMBLE; COMPRISE; SEMICONDUCTOR; CHIP; SUPPORT; CIRCUIT; MECHANICAL; ATTACH; CHIP; SUPPORT; CIRCUIT; EXPOSE; PAD; ELECTROLESS; PLATE; CONTACT; TERMINAL

+=

10/9/11
DIALOG(R)File 350:Derwent **WPIX**

015634702 **Image available**
WPI Acc No: 2003-696884/200366
Using nitrides for flip-chip encapsulation, e.g. for **ball** grid

array
Patent Assignee: AKRAM S (AKRA-I); FARNWORTH W M (FARN-I)
Inventor: AKRAM S; FARNWORTH W M

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030137062	**A1**	**20030724**	**US 96717273**	**A**	**19960920**	**200366 B**
			US 98138038	A	19980820	
			US 2003342798	A	20030113	

Div ex patent US 5956605
Cont of patent US 6528894

Abstract (Basic): US 20030137062 A1

NOVELTY - Manufacturing semiconductor device assembly (40) comprises:

(i) providing semiconductor components with active surface having bond pads (14);

(ii) applying a silicon nitride containing layer (22) over active surface(s) and conductive connector (16);

and

(iii) attaching the revealed segments of conductive connector to terminal pads (44) on a surface of a substrate (12).

USE - For fabricating semiconductor device assembly, e.g. chip on board, **ball** grid array.

ADVANTAGE - The assembly provides simple, quick, and inexpensive formation of hermetic seal on wafer or semiconductor chip without damage to the semiconductor chip or bond pads. It eliminates the possibility of moisture or other contaminants infiltrating.

DESCRIPTION OF DRAWING(S) - The figure shows a side cross-sectional view of the first coated semiconductor assembly.

Flip chip (10)
Substrate (12)
Bond pads (14)
Conductive connector (16)
Silicon nitride containing layer (22)
End portion (32)
Semiconductor device assembly (40)
Carrier substrate (42)
Terminal pads (44)
pp; 12 DwgNo 5/18

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Methods: The silicon nitride containing layer is applied by covering portion(s) of peripheral edge of the semiconductor component bounding the active surface.

The method also comprises applying passivation layer over the semiconductor component and substrate surface, forming and providing conductive connectors as rigid mechanism, **cleaning** the semiconductor component prior to the applying of silicon nitride containing layer, etching a beveled channel around a boundary of the semiconductor chip prior to the applying of silicon nitride containing layer, and dicing the wafer after removing the silicon nitride containing layer.

The conductive connectors are made from reflowable metallic material, conductive **polymer** material, or conductor-carrying **polymer** material. The portion of silicon nitride containing layer is removed by etching the silicon nitride containing layer form an end portion (32) of the conductive connectors at 100-140degreesC. The silicon nitride containing layer portion can also be removed by

abrading a top portion of the silicon nitride containing layer form conductive connectors, or fracturing the silicon nitride containing layer at a top portion of each of the conductive connectors.

The etching process comprises dipping the end portions of the conductive connectors in a phosphoric acid solution. The silicon nitride containing layer is applied by **plasma** enhanced chemical vapor deposition. The etching comprises extending the beveled channel through the integrated circuit layers on the active surface.

Preferred Components: The passivation layer includes a second silicon nitride containing layer. The silicon nitride containing layer is 1-2mum thick. The active surface includes integrated circuitry layers. The semiconductor components comprises wafer with semiconductor chip

Title Terms: FLIP; CHIP; ENCAPSULATE; **BALL**; GRID; ARRAY
Derwent Class: L03; U11
International Patent Class (Main): H01L-023/29
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L04-C12B; L04-F01
Manual Codes (EPI/S-X): U11-D01A3; U11-E02A

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10/9/12
DIALOG(R)File 350:Derwent **WPIX**

015633647 **Image available**
WPI Acc No: 2003-695829/200366

Formation of aluminum **bumps** on semiconductors by **plasma** etching through passivation layer using **polyimide** layer as mask to form **openings** exposing input/output pads, and filling **openings** with metal by chemical vapor deposition technique

Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO LTD (TASE-N)
Inventor: LEE C

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020142575	**A1**	**20021003**	**US 2001821930**	**A**	**20010330**	**200366**	**B**
US 6458683	**B1**	**20021001**	**US 2001821930**	**A**	**20010330**	**200366**	

Abstract (Basic): US 20020142575 A1

NOVELTY - Aluminum **bumps** are formed by **plasma** etching through a passivation layer using **polyimide** layer as a mask to form of **openings** exposing input/output (I/O) pads and filling the **openings** with a metal comprising aluminum by chemical vapor deposition (CVD) technique.

DETAILED DESCRIPTION - Formation of aluminum (Al) **bumps** comprises:

(1) providing a pre- processed semiconductor structure (60) with I/O pads formed on top;

(2) depositing a passivation layer of an insulating material on top of the structure;

(3) printing a **polyimide** layer on top of the passivation layer exposing the portions of passivation layer that overlies the I/O pads;

(4) **plasma** etching through the passivation layer by using **polyimide** layer as a mask to form **openings** exposing the I/O pads;

(5) filling the **openings** with a metal comprising Al by CVD

technique; and
(6) removing the **polyimide** layer and exposing **bumps** comprising Al.
USE - For forming Al **bumps** on semiconductor devices.
ADVANTAGE - The invented method has reduced processing steps than that of conventional process, thus reducing time and labor costs. It also achieves good profile control with minimal residue problems, and no Al etching is required. The process requires only one photolithographic step.
DESCRIPTION OF DRAWING(S) - The figure is an enlarged, cross-sectional view of the semiconductor structure.
pp; 10 DwgNo 3A/3
Technology Focus:
TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The method further comprises forming I/O pads in a metal comprising Al.
The passivation layer is deposited from silicon oxide, silicon nitride (Si3N4) or spin-on-glass. It also deposited in at least two sublayers of a first layer of Si3N4 in a thickness of 5000-8000 Angstrom and a second layer of silicon dioxide of 2000-4000 Angstrom. The passivation layer is deposited to a thickness of at least 1 micron.
A metal comprising Al and copper is deposited by CVD into the **opening**. The **polyimide** layer is removed by wet etch using an etchant comprising hydrogen fluoride and ammonium fluoride. It is printed by screen or stencil printing.
POLYMERS - Preferred Method: The **polyimide** layer is deposited to a thickness of at least 5, preferably 5-10 microns. It is printed by screen or stencil printing.
Alternatively, the **polyimide** layer is removed by wet etch using an etchant comprising hydrogen fluoride and ammonium fluoride.
Title Terms: FORMATION; ALUMINIUM; **BUMP**; SEMICONDUCTOR; **PLASMA**; ETCH; THROUGH; PASSIVATION; LAYER; **POLYIMIDE**; LAYER; MASK; FORM; **OPEN**; EXPOSE; INPUT; OUTPUT; PAD; FILL; **OPEN**; METAL; CHEMICAL ; VAPOUR; DEPOSIT; TECHNIQUE
Derwent Class: A85; L03; U11
International Patent Class (Main): H01L-021/283; H01L-021/44
File Segment: CPI; EPI
Manual Codes (CPI/A-N): A05-J01B; A11-C04A; A11-C04D; A12-E07C; L04-C07D
Manual Codes (EPI/S-X): U11-C05C3; U11-C05G2B; U11-C07A1; U11-C07D1

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DIALOG(R)File 350:Derwent **WPIX**

015468860 **Image available**
Conductive trace connection method for semiconductor chip assembly, involves forming connection joint in through-**hole**, to electrically connect conductive trace and conductive pad
Patent Assignee: LIN C W C (LINC-I)
Inventor: LIN C W C

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6440835	**B1**	**20020827**	**US 2000687619**	**A**	**20001013**	**200350**	**B**

Abstract (Basic): US 6440835 B1
NOVELTY - A conductive pad (16) on a chip (10) is aligned with a through-**hole** in a conductive trace (32). A base that is made of a material different from that of the trace, covers the through-

hole on a side opposing the chip. A portion of the base is removed, so as to expose the through-**hole**. A connection joint (52) that electrically connects the trace and pad, is formed in the through-**hole**.

USE - For connecting a conductive trace through a semiconductor chip in semiconductor chip assembly such as **ball** grid array (BGA) semiconductor packages, land grid array (LGA) semiconductor packages.

ADVANTAGE - By forming the connection joint to electrically connect the conductive trace and pad, the chip assembly without any **solder** joints is formed, using low temperature processes that reduces stress and improves reliability.

DESCRIPTION OF DRAWING(S) - The figure shows an enlarged cross-sectional view illustrating connection joint formation.

Chip (10)
Conductive pad (16)
Conductive trace (32)
Connection joint (52)
pp; 44 DwgNo 4E/7

Technology Focus:

TECHNOLOGY FOCUS - **POLYMERS** - Preferred Component: The adhesive provided to the conductive trace, base and the chip comprises thermosetting epoxy, thermoplastic **polyimide**.

Title Terms: CONDUCTING; TRACE; CONNECT; METHOD; SEMICONDUCTOR; CHIP; ASSEMBLE; FORMING; CONNECT; JOINT; THROUGH; **HOLE**; ELECTRIC; CONNECT ; CONDUCTING; TRACE; CONDUCTING; PAD
Derwent Class: A85; L03; U11
International Patent Class (Main): H01L-021/44
File Segment: CPI; EPI
Manual Codes (CPI/A-N): A05-A01E2; A05-J01B; A12-E04; A12-E07C; L04-C13
Manual Codes (EPI/S-X): U11-C05D4; U11-D01A3; U11-D01A5

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10/9/15
DIALOG(R)File 350:Derwent **WPIX**

015429545 **Image available**
WPI Acc No: 2003-491687/200346

Conductive preform placement method for **ball** grid array applicator, comprises holding preforms in **openings** of foil against porous layer partially covering portion of **openings**

Patent Assignee: GALAHAD CO (GALA-N)
Inventor: HERTZ E L

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6510977	**B1**	**20030128**	**US 97789883**	**A**	**19970128**	**200346**	**B**
			US 2000680526	A	20001002		
			CIP of patent US 6202918				
			Cont of patent US 6230963				

Abstract (Basic): US 6510977 B1

NOVELTY - The conductive preforms (320) are held partially within the **openings** (322) of exposed diameter equal to or larger than the diameter of preforms in à foil (310) against porous layer (340) which partially covers a portion of **openings**. The preforms are placed on the electronic pads by removing the vacuum force (222) applied to the preforms.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the

following:
(1) apparatus for placing conductive preforms; and
(2) method of placing pattern of **solder** spheres.
USE - For placing conductive preforms e.g. **solder balls**, **solder** spheres and preformed **solder bumps** on electronic pads for **ball** grid array applicator.
ADVANTAGE - Does not require any additional forces for releasing preforms, thus very simple, repeatable and low cost processing is achieved. The conductive preforms are placed on different patterns of pads and the placed pattern of preforms can be modified by filling or covering undesirable apertures. The porous layer increases the reliability of the filler material.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of foil and block structure.
vacuum force (222)
foil (310)
conductive preforms (320)
openings (322)
porous layer (340)
pp; 15 DwgNo 3/14

Technology Focus:
TECHNOLOGY FOCUS - METALLURGY - Preferred Material: The foil is selected from the group consisting of stainless steel, brass, nickel, **polyimide** and **polyester** film.
INORGANIC CHEMISTRY - Preferred Material: The porous layer consists of materials such as woven fabric, **polyester** mesh, silk screen, metal screening and sponge-type material.

Title Terms: CONDUCTING; PREFORM; PLACE; METHOD; **BALL**; GRID; ARRAY; APPLY; COMPRISE; HOLD; PREFORM; **OPEN**; FOIL; POROUS; LAYER; COVER; PORTION; **OPEN**
Derwent Class: A88; P55; U11; V04; X24
International Patent Class (Main): B23K-001/08
International Patent Class (Additional): B23K-005/00; B23K-020/14; B23K-035/12
File Segment: CPI; EPI; EngPI
Manual Codes (CPI/A-N): A12-E07A; A12-H
Manual Codes (EPI/S-X): U11-C05G2B; U11-D01A3; U11-D03B1; V04-R04A5A; X24-A01C; X24-A09

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10/9/17
DIALOG(R)File 350:Derwent **WPIX**

015041151 **Image available**
Manufacture of flip-chip device includes sequentially applying conductive non-wettable layer, wettable stud and **solder bump** over copper structure on semiconductor chip
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: MARLIN G W

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6429046	**B1**	**20020806**	**US 2000615865**	**A**	**20000713**	**200309**	**B**

Abstract (Basic): US 6429046 B1
NOVELTY - A flip-chip device is manufactured by providing a power copper (104) formed over a semiconductor chip (102); applying a

conductive non-wettable layer (302) over the power copper; applying a wettable stud (308) over the non-wettable layer; and applying a **solder bump** (310) to the wettable stud.

USE - For manufacturing a flip-chip device (claimed).

ADVANTAGE - The **solder bump** will not collapse and will stay in a proper configuration under heating and reflowing. The materials used for the non-wettable layer will not dissolve the power copper, which can occur when **polyimide** layers are used.

DESCRIPTION OF DRAWING(S) - The figure illustrates the flip chip device at the final stage of manufacture.

Semiconductor chip (102)
Adherence layer (103)
Power copper (104)
Non-wettable layer (302)
Stud (308)
Solder bump (310)
pp; 5 DwgNo 6/6

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Process: The non-wettable layer is applied by sputtering a conductive layer; sputtering a copper layer over the conductive layer; depositing a photoresist layer over the copper layer; using a mask and developing the mask image to remove the photoresist layer from everywhere except over a portion of the power copper; removing the copper layer from all exposed areas; and removing the remaining photoresist. The **solder bump** is applied by coating the device with photoresist; forming an **opening** in the photoresist over the power copper; plating a copper stud; plating **solder** on the copper stud; stripping the photoresist; and etching the conductive layer and the copper layer. Further, an adherence layer (103) is provided between the power copper and the semiconductor chip.

METALLURGY - Preferred Materials: The non-wettable layer is made up of titanium-tungsten, while the **solder bump** is made up of lead-tin.

Title Terms: MANUFACTURE; FLIP; CHIP; DEVICE; SEQUENCE; APPLY; CONDUCTING; NON; WET; LAYER; WET; STUD; **SOLDER**; **BUMP**; COPPER; STRUCTURE; SEMICONDUCTOR; CHIP

Derwent Class: L03; U11

International Patent Class (Main): H01L-021/44

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10/9/18

DIALOG(R)File 350:Derwent **WPIX**

014910109 **Image available**

WPI Acc No: 2002-730815/200279

Production of semiconductor chip assembly, e.g. chip size package, involves etching conductive metal to provide through-**hole**, and forming connection joint in the through-**hole** to connect the conductive metal to conductive pad

Patent Assignee: LIN C W C (LINC-I)

Inventor: LIN C W C

Patent No	Kind	Date	Applicat No	Kind	Date	Week

US 6448108 B1 20020910 US 2000677207 A 20001002 200279 B

Abstract (Basic): US 6448108 B1

NOVELTY - A semiconductor chip assembly is produced by providing a semiconductor chip which includes a conductive pad, and a conductive metal forms from a single metallic material that includes a dimple; etching the metal on a side opposite the dimple such that the dimple forms a through-**hole**; and forming a connection joint in the through-**hole** that connects the conductive metal and the pad.

USE - The method is for producing a semiconductor chip assembly, e.g. chip size package (claimed), or **ball** grid arrays.

ADVANTAGE - The inventive method provides semiconductor chip assembly that is cost-effective, high performance, high reliability, manufacturable, has excellent mechanical and electrical performance, and complies with stringent environmental standards. Specifically, the chip assembly is devoid of wire bond, TAB leads, or **solder** joints. It can be manufactured using low temperature processes that reduces stress and improves reliability. It is produced using a well-controlled wet chemical processes that can be easily implemented by circuit board, lead frame, and tape manufacturers; or using materials that are compatible with copper chips and lead-free environmental requirements.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a semiconductor chip assembly.

Chip assembly (10)
Routing line (30)
Adhesive (40)
Pillar (50)
Connection joint (60)
Insulative base (62)
pp; 47 DwgNo 1N/6

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The chip assembly (10) is attached to the conductive metal by an adhesive (40) before forming the through-**hole**. An **opening** is formed in the adhesive directly below the through-**hole**, thus exposing the pad after attaching the chip to the metal. It is formed by laser etch, or by removing the adhesive in the through-**hole**. The laser etch includes projection laser ablation. The dimple is formed by etching the conductive metal. The metal is also etched to form a pillar (50). The connection joint (60) is formed before or after forming the pillar. It is formed by plating metal on the conductive metal and the pad. The conductive metal is partially etched to provide outer edges of a routing line (30). The chip is encapsulated after attaching the chip to the conductive metal and before etching the metal. An insulative base (62) is form over the routing line, the through **hole**, and a lower portion of the pillar.

Preferred Component: The pad includes a central region and peripheral region. The **opening** and the through-**hole** expose the central region without exposing the peripheral region. The connection joint contacts the central region without contacting the peripheral region. The pillar has a flat, and narrowest diameter at top surface.

Preferred Property: The pillar extends at at least 100 microns above the insulative base.

INORGANIC CHEMISTRY - Preferred Material: The conductive metal is copper.

POLYMERS - Preferred Material: The insulative base is epoxy
Title Terms: PRODUCE; SEMICONDUCTOR; CHIP; ASSEMBLE; CHIP; SIZE; PACKAGE; ETCH; CONDUCTING; METAL; THROUGH; **HOLE**; FORMING; CONNECT; JOINT; THROUGH; **HOLE**; CONNECT; CONDUCTING; METAL; CONDUCTING; PAD
Derwent Class: A85; L03; U11
International Patent Class (Main): H01L-021/44
File Segment: CPI; EPI

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10/9/19
DIALOG(R)File 350:Derwent **WPIX**

014715338 **Image available**
WPI Acc No: 2002-536042/200257
Manufacture of semiconductor chip assembly involves mechanically attaching the chip to support circuit such that base covers portion of conductive trace and pad directly beneath the conductive trace
Patent Assignee: LIN C W C (LINC-I)
Inventor: LIN C W C

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6403460	**B1**	**20020611**	**US 2000643445**	**A**	**20000822**	**200257**	**B**

Abstract (Basic): US 6403460 B1

NOVELTY - A semiconductor chip assembly is manufactured by mechanically attaching the chip to a support circuit such that the base covers a portion of a conductive trace and a portion of pad (216) directly beneath the conductive trace.

DETAILED DESCRIPTION - Manufacture of a semiconductor chip assembly involves providing a semiconductor chip that includes a conductive pad; providing a support circuit that includes an insulative base and a conductive trace; mechanically attaching the chip to the support circuit such that the base covers a portion of the conductive trace and a portion of the pad directly beneath the conductive trace; and applying an etch to form an **opening** in the base that exposes the conductive trace and the pad.

USE - For manufacture of semiconductor chip assembly.

ADVANTAGE - The invention provides a low cost, high performance, high reliability package. It also provides a convenient, cost-effective method for manufacturing semiconductor chip assembly. The semiconductor assembly need not include wire bonds, tape automated bonding leads or **solder** joints. It can be manufactured using low temperature processes which reduces stress, and by using well-controlled wet chemical processes which can be easily implemented by circuit board, lead frame, and tape manufacturers. It can be manufactured using materials that compatible with copper chip and lead-free environmental requirements.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of manufacturing a semiconductor chip assembly.

Pad (216)
Insulative base (226)
Routing line (234)
Adhesive (240)
pp; 21 DwgNo 3D/9

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The etch is applied by directing a laser at the base. The chip is mechanically

attached to the support circuit by disposing an insulative adhesive (240) between the chip and the support circuit, and applying the etch forms an **opening** in the adhesive directly beneath the **opening** in the base, thus exposing the conductive trace through the **openings** in the base and the adhesive. A connection joint is formed in the **opening** that contacts and electrically connects the conductive trace and the pad. The connection joint contacts a surface of the conductive trace that is disposed above and overlaps and faces away from the pad.

Preferred Component: The conductive trace includes a pillar and a routing line (234). The pillar extends above the base and is horizontally spaced from the pad, and the routing line extends below the base and extends above and overlaps the pad. The conductive trace overlaps only one peripheral edge of the pad. The assembly is a chip scale package. The pillar extends at least 100 microns above the base.

INORGANIC CHEMISTRY - Preferred Component: The conductive trace a metal from is copper (preferably), gold nickel, palladium, and/or tin.

POLYMERS - Preferred Component: The insulative base (226) is epoxy (tape), silicone or tape.

METALLURGY - Preferred Component: The conductive trace is alloy.

CERAMICS AND GLASS - Preferred Component: The base is glass or ceramic

Title Terms: MANUFACTURE; SEMICONDUCTOR; CHIP; ASSEMBLE; MECHANICAL; ATTACH ; CHIP; SUPPORT; CIRCUIT; BASE; COVER; PORTION; CONDUCTING; TRACE; PAD; BENEATH; CONDUCTING; TRACE

Derwent Class: A85; L03; U11

International Patent Class (Main): H01L-021/44

International Patent Class (Additional): H01L-021/4763; H01L-021/48; H01L-021/50; H01L-023/48; H01L-023/52; H01L-029/40

File Segment: CPI; EPI

Manual Codes (CPI/A-N): A99-A; L04-C07; L04-C17

Manual Codes (EPI/S-X): U11-D03B; U11-E02A2; U11-E02A3

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10/9/21

DIALOG(R)File 350:Derwent **WPIX**

014188529 **Image available**

WPI Acc No: 2002-009226/200201

Testing and packaging of semiconductor chip having integrated circuit and bonding pad, involves electrically testing integrated circuit before forming passivation layer having **opening** for wire bonding or **bumping**

Patent Assignee: UNITED MICROELECTRONICS CORP (UNMI-N)

Inventor: HUANG Y; LIU H

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6251694	**B1**	**20010626**	**US 99318597**	**A**	**19990526**	**200201**	**B**

Abstract (Basic): US 6251694 B1

NOVELTY - A semiconductor chip, having an integrated circuit (IC) and a bonding pad, is tested and packaged by electrically testing first the IC using a probe that contacts a predetermined testing area on the surface of the bonding pad, before forming a passivation layer. The passivation layer has an **opening,** which is used as a connecting area for performing wire bonding or **bumping**.

DETAILED DESCRIPTION - Testing and packaging of semiconductor chip (30), having an integrated circuit (IC) positioned within the chip and a bonding pad (32) positioned on the surface of the chip, includes electrically testing the IC using a probe that contacts a predetermined testing area (34) on the surface of the bonding pad. The bonding pad is electrically connected to the IC. A passivation layer (40) is then formed on the surface of the chip. It comprises an **opening** (46) positioned on the bonding pad outside the testing area, which is used as a connecting area (36) for performing wire bonding or **bumping**.

USE - For testing and packaging of semiconductor chip including an integrated circuit and a bonding pad.

ADVANTAGE - The inventive method allows the testing area to be distinct from the connecting area, thus the peeling of the metal of the bonding pad caused by the probe mark (38) can be avoided.

DESCRIPTION OF DRAWING(S) - The figures are schematic diagram and top view illustrating the testing and packaging of the semiconductor chip.

Semiconductor chip (30)
Bonding pad (32)
Testing area (34)
Connecting area (36)
Probe mark (38)
Passivation layer (40)
Opening (46)
pp; 9 DwgNo 9, 10/12

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The **opening** is formed by performing photolithographic and dry etching processes. This dry etching process is performed by injecting at a low pressure a mixed gas comprising sulfur hexafluoride (SF_6), fluoroform (CHF_3), and carbon tetrafluoride (CF_4). Preferred Component: The bonding pad comprises a glue layer formed from titanium positioned on the surface of the semiconductor chip, an aluminum alloy layer positioned on the glue layer, and an anti-reflection layer of titanium nitride positioned on the surface of the aluminum alloy layer. The passivation layer comprises an inorganic passivation layer positioned on the surface of the semiconductor chip and an organic passivation layer positioned on the inorganic passivation layer.

METALLURGY - Preferred Composition: The aluminum alloy layer contains copper and 95 weight% aluminum.

INORGANIC CHEMISTRY - Preferred Material: The inorganic passivation layer is formed from silicon nitride.

CERAMICS AND GLASS - Preferred Material: The inorganic passivation layer can also be formed from phosphosilicate glass (PSG).

POLYMERS - Preferred Material: The organic passivation layer is formed from **polyimide**.

Title Terms: TEST; PACKAGE; SEMICONDUCTOR; CHIP; INTEGRATE; CIRCUIT; BOND; PAD; ELECTRIC; TEST; INTEGRATE; CIRCUIT; FORMING; PASSIVATION; LAYER; **OPEN**; WIRE; BOND; **BUMP**

Derwent Class: A85; L03; M26; U11

International Patent Class (Main): H01L-031/26

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10/9/22

DIALOG(R)File 350:Derwent **WPIX**

014130407 **Image available**
WPI Acc No: 2001-614617/200171
Semiconductor device comprises electrically conductive redistribution patterns, each of redistribution patterns including **bump** pad area, which includes concave pattern, and including chip pad contact portion connected to associated chip pad
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU); HWANG C S (HWAN-I); JUNG S O (JUNG-I)
Inventor: HWANG C S; JUNG S U; CHUNG S W; JUNG S O

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2001029196	A	20010406	KR 9941883	A	19990930	200171	B
US 6621164	**B2**	**20030916**	**US 2000672379**	**A**	**20000928**	**200402**	
KR 306842	B	20011102	KR 9941883	A	19990930	200238	
US 6455408	**B1**	**20020924**	**US 2000672379**	**A**	**20000928**	**200266**	
US 20020185721	**A1**	**20021212**	**US 2000672379**	**A**	**20000928**	**200301**	
			US 2002209344	A	20020730		

Abstract (Basic): US 6621164 B2

NOVELTY - A semiconductor device (90) comprises electrically conductive redistribution patterns (64) formed on a first barrier metal layer (70), each of the redistribution patterns including a **bump** pad area, which includes a concave pattern, and including a chip pad contact portion that is electrically connected to an associated chip pad (54).

DETAILED DESCRIPTION - A semiconductor device comprises a semiconductor integrated circuit chip having a semiconductor substrate (52), chip pads, and a passivation layer (56) positioned on a surface of the semiconductor substrate, the passivation layer including **openings** to expose the chip pads; a first **polymer** layer (58) formed on the passivation layer and having first **openings** for exposing the chip pads; a patterned first barrier metal layer formed on the chip pads and the first **polymer** layer; and electrically conductive redistribution patterns formed on the first barrier metal layer, each of the redistribution patterns including a **bump** pad area, which includes a concave pattern, and including a chip pad contact portion that is electrically connected to an associated chip pad.

USE - Used as semiconductor device, e.g. chip size package.

ADVANTAGE - The concave pattern in the **bump** pad increases the joint area between the **solder bump** and the **bump** pad, and improves the adhesive strength reliability of the **solder** joint. Since the concave pattern is formed simultaneously with forming the redistribution pattern, additional equipment or process is not required, and there is no increase in production cost.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional or plan view of portions of a semiconductor wafer illustrating the manufacture of a chip size package.

Semiconductor substrate (52)
Chip pad (54)
Passivation layer (56)
First **polymer** layer (58)
Electrically conductive redistribution patterns (64)
Barrier metal layer (70)
Second **polymer** layer (74)

Solder bump (80)
Semiconductor device (90)
pp; 15 DwgNo 17/19

Technology Focus:

TECHNOLOGY FOCUS - **POLYMERS** - Preferred Component: A second **polymer** layer (74) is formed on the first **polymer** layer and the redistribution patterns, and having a second **openings**, one for each **bump** pad area.

ELECTRONICS - Preferred Component: The semiconductor device comprises a second baffler metal layer formed on each of the redistribution patterns; a **solder bump** (80) positioned on each of the **bump** pad areas and extending into the concave pattern of each **bump** pad area; and a third baffler metal layer positioned in each of the **bump** pad areas, and interposed between the second barrier metal and a portion of the **solder bump**. Preferred Parameter: An area of the concave pattern is approximately10-50% of the area of the **bump** pad. The concave pattern includes a side wall, which is inclined at an angle of approximately45-90degrees, to a surface of one of the redistribution patterns.

Title Terms: SEMICONDUCTOR; DEVICE; COMPRISE; ELECTRIC; CONDUCTING; REDISTRIBUTE; PATTERN; REDISTRIBUTE; PATTERN; **BUMP**; PAD; AREA; CONCAVE; PATTERN; CHIP; PAD; CONTACT; PORTION; CONNECT; ASSOCIATE; CHIP; PAD

Derwent Class: A85; U11

International Patent Class (Main): H01L-021/28; H01L-021/44; H01L-021/60; H01L-023/48

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10/9/24

DIALOG(R)File 350:Derwent **WPIX**

014094370 **Image available**

WPI Acc No: 2001-578584/200165

Mounting of **ball** grid array chip, involves combination of build up multi-layer equipment and thin film deposition equipment in creating thin film layer on metal substrate

Patent Assignee: THIN FILM MODULE INC (THIN-N)

Inventor: HO C W; LITZA A

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6242279	**B1**	**20010605**	**US 99332428**	**A**	**19990614**	**200165**	**B**

Abstract (Basic): US 6242279 B1

NOVELTY - A **ball** grid array (BGA) chip is mounted by creating a thin film layer (32-36) over a metal substrate (14) by using a combination of build up multi-layer (BUM) equipment and thin film deposition equipment. **Openings** are then created in the metal for insertion of the BGA chip (16) and BGA contact **balls** (10, 11).

DETAILED DESCRIPTION - Mounting a BGA chip comprises creating a thin film layer over a first surface of a metal substrate. The thin film is created by using a combination of printed wiring board equipment (e.g. plating and wet etch), BUM equipment (e.g. a dielectric coater and laser via) and thin film deposition equipment (e.g. a sputter or a projection printer). The metal pads within the first surface of the thin film layer are exposed to create **openings** for wire bond connections in addition to BGA **solder** connections. The first surface of the substrate is milled to create an **opening** for

the insertion of the BGA chip. After inserting the BGA chip, bond wires (38) are connected between the BGA chip and the **openings** for the wire bond connections, and BGA contact **balls** are inserted into the **openings** for the BGA **solder** connections. The BGA device is heat-treated to establish electrical contacts between the BGA contact **balls** and the first surface of the thin film layer. The substrate is then subdivided into individual BGA substrates.

USE - The method is used for mounting a BGA chip, and also for mounting land grid array chip or pin grid array chip.

ADVANTAGE - The inventive method is inexpensive and reliable, and reduces performance limitations imposed by prior art techniques. It provides high pin fan-out and increased power dissipation for semiconductor devices.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of a multi-chip BGA with three layers of patterned metal.

BGA contact **balls** (10, 11)
Metal substrate (14)
BGA chip (16)
Thin film layers (32-36)
Bond wires (38)
pp; 9 DwgNo 3/6

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The thin film layer is created by **cleaning** the first surface of the metal substrate and treating the surface with an adhesion promotion step, e.g. an oxidation growth step. The metal substrate is then coated with a dielectric layer by lamination techniques or coating and curing techniques. Vias are created in the dielectric layer for electrical connections to the metal substrate. An interconnect plating base is sputter-deposited over the dielectric layer by depositing a first chromium layer, a first copper layer, and a second chromium layer. A photoresist layer is then deposited over the interconnect plating base, and masked to create a photoresist mask. The second chromium layer is etched to expose portions of the underlying first copper layer. A semi-additive plating is formed on the exposed portions of the first copper layer by depositing a second copper layer, a nickel layer and a gold layer. The photoresist mask is then removed to expose portions of the interconnect plating base, and the exposed portions are etched to form an interconnect pattern comprising the interconnect plating base and the semi-additive plating. The metal pads are exposed by using a laser technology, thus creating laser vias. The first surface of the metal substrate is milled by mechanical milling or by etchback. Preferred Dimensions: The thickness of the dielectric layer is 10-40 mum, while that of the metal substrate is 40 mils. The planar dimensions of the metal substrate are large enough to provide for one or more surfaces, each having dimensions of 18x24 inches.

INORGANIC CHEMISTRY - Preferred Material: The metal substrate is copper or aluminum.

METALLURGY - Preferred Material: The metal substrate can also be stainless steel.

POLYMERS - Preferred Material: The dielectric layer comprises epoxy (with or without glass reinforcement) and/or **polyimide**.

Title Terms: MOUNT; **BALL**; GRID; ARRAY; CHIP; COMBINATION; BUILD; UP; MULTI; LAYER; EQUIPMENT; THIN; FILM; DEPOSIT; EQUIPMENT; THIN; FILM; LAYER; METAL; SUBSTRATE

Derwent Class: L03; U11; U14

International Patent Class (Main): H01L-021/48
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L04-C17A
Manual Codes (EPI/S-X): U11-D01A3; U11-E02A3; U14-H01F

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10/9/30
DIALOG(R)File 350:Derwent **WPIX**

013421446 **Image available**
WPI Acc No: 2000-593385/200056
Packaging wafer scale includes forming a **polymeric** body having metal posts that can bend to absorb the stress due to the thermal mismatch between the semiconductor wafer and the **polymeric** body
Patent Assignee: LIN M (LINM-I)
Inventor: LIN M

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6103552	**A**	**20000815**	**US 98131429**	**A**	**19980810**	**200056**	**B**
TW 425645	A	20010311	TW 99111047	A	19990630	200143	

Abstract (Basic): US 6103552 A

NOVELTY - A wafer scale is packaged by providing a semiconductor wafer having chip images separated by a kerf area and has a topmost passivating layer through which connecting studs pass; forming a **polymeric** body having metal posts fixed to the connecting studs. The posts can bend to absorb the stress due to the thermal mismatch between the semiconductor wafer and the **polymeric** body.

DETAILED DESCRIPTION - The wafer scale is packaged by providing a semiconductor wafer that includes chip images separated by a kerf area and has a topmost passivating layer through which connecting studs pass; and forming a **polymeric** body having metal posts in contact with and fixed to the connecting studs and passing vertically through the **polymeric** body from the studs. The posts can bend to absorb the stress due to the thermal mismatch between the semiconductor wafer and the **polymeric** body.

USE - For packaging semiconductor chips.

ADVANTAGE - The process does not require any special jigs or fixtures for its implementation and provides packages that are cheaper than those obtained through individual chip packaging processes. It is also suitable for packages having a high density of interconnections.

DESCRIPTION OF DRAWING(S) - The figure shows the formation of the **solder ball.**

Polymeric body (51)

Solder bumps (71)

pp; 12 DwgNo 7a/13

Technology Focus:

TECHNOLOGY FOCUS - **POLYMERS** - Preferred Material: The **polymeric** body is a **polyimide**, a silicone elastomer or **benzocyclobutene.**

ELECTRONICS - Preferred Method: The method further comprises (a) forming via **holes** using chemical etching or laser drilling in the **polymeric** body where conduct posts are formed; (b) using a photosensitive version of the **polymeric** material, having an upper and lower surface, that provides a positive image of the mask; (c) employing an imaging system that has a low depth of focus; (d) focusing

in a plane midway between the surfaces, causing the via **holes** to be narrowed to a point halfway down the **holes;** (e) etching back the layer of **polymeric** material to generate a lollipop structure from the post and **solder bump** combination; and (f) coating the uncovered portions of the post before forming the **solder bumps**. The step of forming via **holes** further comprises using a photoresist mask in conjunction with a hard mask over the **polymeric** material and then etching the **polymeric** material. Preferred Property: The bending force exerted at the free end of the metal post having a length L displaced by an amount d, is according to a formula, F=(3YId)/L3, where Y=Young's modulus and I=moment of inertia. The **polymeric** body (51) and the metal layers have a thickness of 20-250mum. The posts project 10-75mum above the layer of **polymeric** material. Preferred Component: The via **holes** further comprise a photosensitive version of the **polymeric** material which is exposed through a mask and developed to form the **holes**. The via **holes** are formed by chemical etching or by laser drilling.

INORGANIC CHEMISTRY - Preferred Component: The metal layer consists of copper, gold, **solder,** or aluminum.

IMAGING AND COMMUNICATION - Preferred Method: The **solder bumps** (71) are laid down using screen printing stenciling.

CHEMICAL ENGINEERING - Preferred Component: The metal posts are formed by electroplating or by electroless plating. The **polymeric** body is laid down by spin coating, dipping, spraying, or in the form of a dry film with an adhesive undercoating.

Title Terms: PACKAGE; WAFER; SCALE; FORMING; **POLYMERISE**; BODY; METAL; POST; CAN; BEND; ABSORB; STRESS; THERMAL; MISMATCH; SEMICONDUCTOR; WAFER; **POLYMERISE**; BODY

Derwent Class: A32; A85; L03; U11

International Patent Class (Main): H01L-021/44; H01L-021/60

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10/9/38

DIALOG(R)File 350:Derwent **WPIX**

012202649 **Image available**

WPI Acc No: 1999-008755/199901

Fabricating micro-**bump** interconnect for semiconductor dice - involves depositing metal in **openings** in mask onto conductors formed on **polymer** layer

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)

Inventor: AKRAM S

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5834366	**A**	**19981110**	**US 96647749**	**A**	**19960515**	**199901**	**B**

Abstract (Basic): US 5834366 A

An interconnect is fabricated by forming conductors on an electrically insulating **polymer** on a substrate, forming a mask on the substrate with **openings** to the conductors corresponding to a pattern of contacts on a die, forming microbumps on the conductors by depositing metal in the **openings** and configured to electrically engage the contacts and flex with the **polymer** layer to accommodate dimensional variations in the microbumps and contacts, and removing the mask.

USE - In the fabrication of a multichip module, and in the fabrication of a test assembly for a semiconductor die (both claimed).

ADVANTAGE - A temporary or permanent electrical connection to a bare semiconductor die can be made. The microbumps have low resistance.

Dwg.1d/6

Title Terms: FABRICATE; MICRO; **BUMP**; INTERCONNECT; SEMICONDUCTOR; DICE; DEPOSIT; METAL; **OPEN**; MASK; CONDUCTOR; FORMING; **POLYMER**; LAYER

Derwent Class: A85; L03; U11

International Patent Class (Main): H01L-021/44

File Segment: CPI; EPI